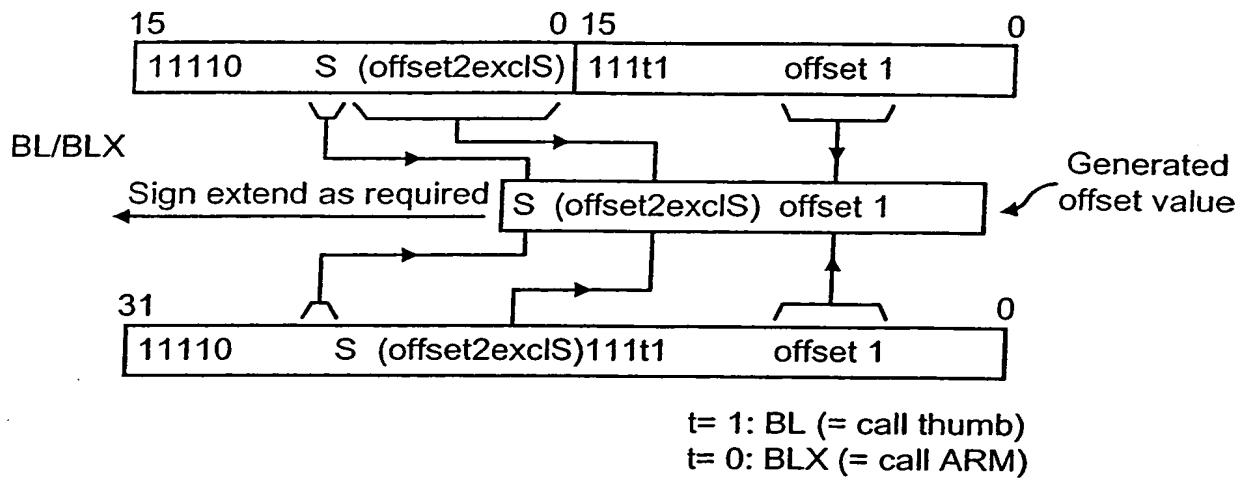
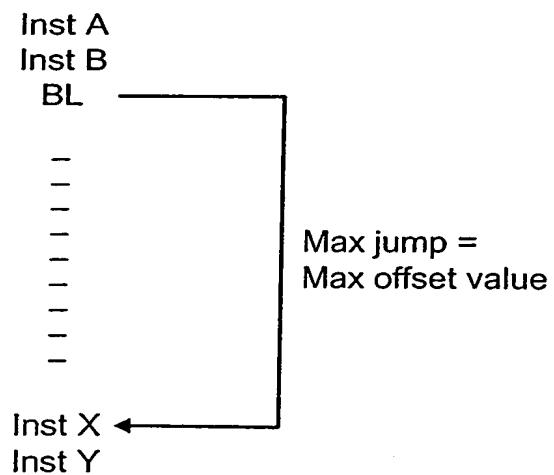


FIG. 1

PRIOR ART

**FIG. 2**

PRIOR ART

**FIG. 3**

PRIOR ART

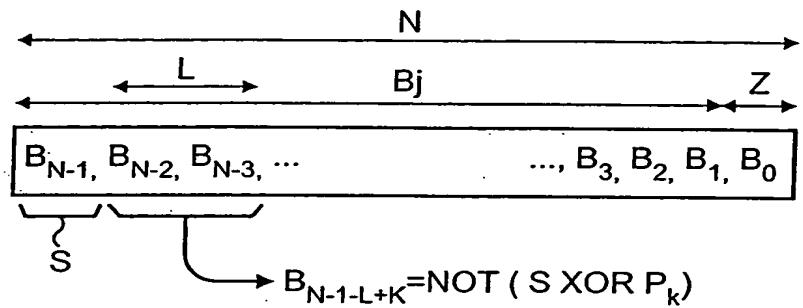


FIG. 4

Address
offset generating
instruction

11110 S {offset[N-4:M]}	11P ₁	tp ₀	{offset[M-1 : Z]}
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FIG. 5

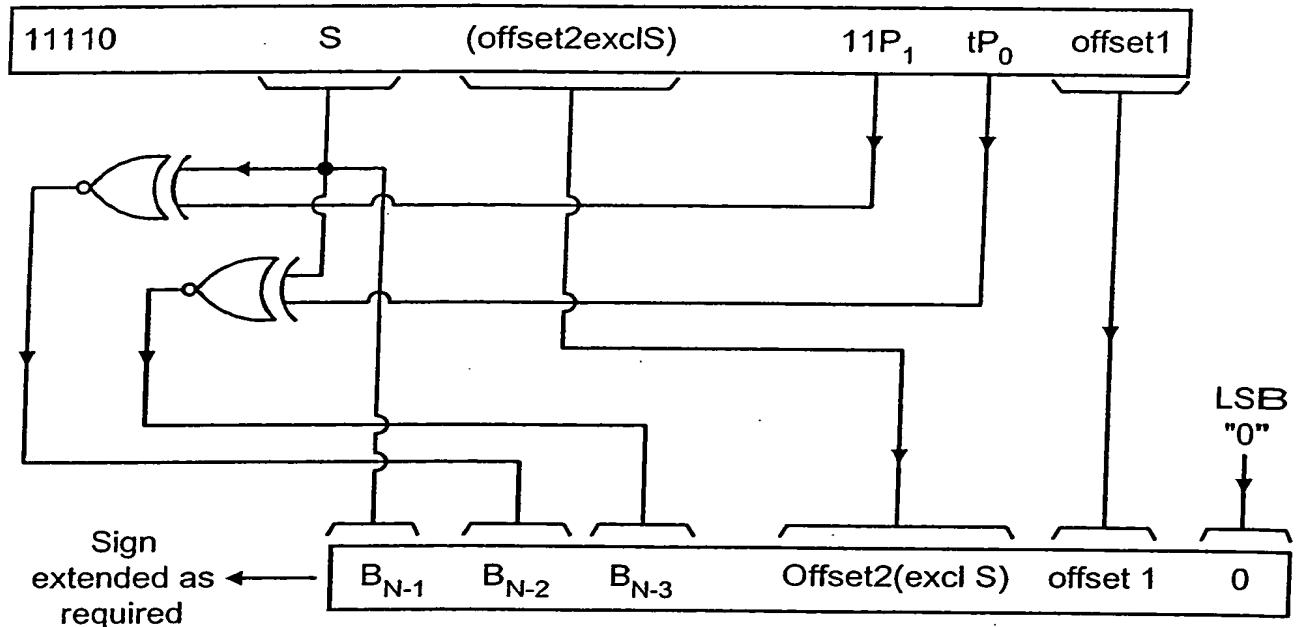


FIG. 6

S	P ₁	P ₀	B _{N-1}	B _{N-2}	B _{N-3}
0	0	0	-	A	-
0	0	1	-	B	-
0	1	0	-	C	-
0	1	1	0	0	0
1	0	0	-	D	-
1	0	1	-	E	-
1	1	0	-	F	-
1	1	1	1	1	1

{A,B,C,D,E,F} is a permutation of
{001,010,011,100,101,110}

FIG. 7

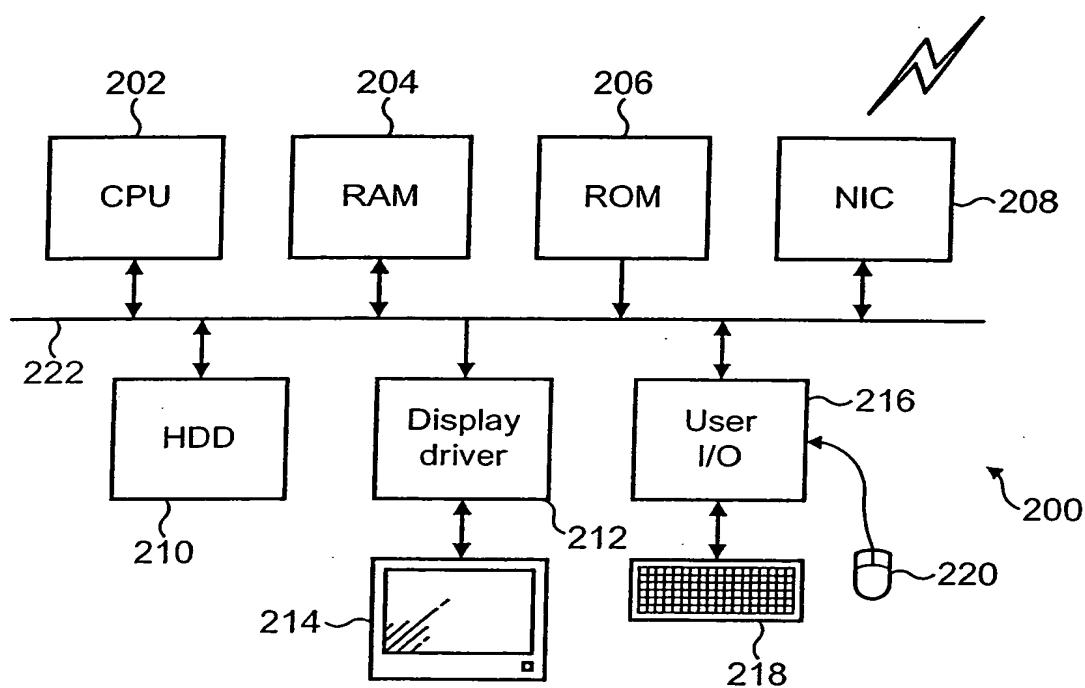


FIG. 8